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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/534,462	05/11/2005	Daniel Chatroux	123886	5027

25944 7590 04/25/2008

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EXAMINER	
MEMULA, SURESH	
ART UNIT	**PAPER NUMBER**
2825	

MAIL DATE	DELIVERY MODE
04/25/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/534,462	CHATROUX ET AL.	
	Examiner	Art Unit	
	SURESH MEMULA	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This FINAL office action is supplemental to the final action mailed on 10/25/2007 and in response to and necessitated by the after-final amendments and remarks filed on 02/25/2008. The rejections under Myono et al. are withdrawn; however, this case is not in condition for allowance in view of the newly found art detailed below. Claims 17-30 are pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 17-25 and 27 are rejected under 35 U.S.C. 102(b)** as being anticipated by US Pub. No. 2002/0125933 to Tamura et al. (Tamura).

3. As to claim 17,

an integrated circuit (FIG. 8, element 4) comprising at least a digital part comprising a plurality transistors connected to one another so as to form a plurality of functional elements (FIG. 8, elements 44-47),

the functional elements being grouped in subassemblies (FIG. 8: elements 44-45 and 46-47) each comprising a first and a second electrical supply terminal (FIG. 8: Vdd and Vss) and a clock input (FIG. 8: element SS; SS is a clock signal as evidenced by the waveforms of FIG. 1 and 2),

the subassemblies being connected in series by means of their supply terminals to the terminals of a voltage supply source (FIG. 8),

wherein a same clock signal is applied to the clock input of all subassemblies by means of a device for shifting the levels of the clock signals (FIG. 8: element SS; FIG. 1-2 and 7),

wherein the subassemblies are formed in such a way that the same current flows through the different subassemblies (FIG. 8: Elements 44-47 are connected in series, so the current flowing through elements 44-45 and elements 46-47 are the same.).

4. As to Claim 18, wherein the clock inputs of at least two adjacent subassemblies are connected by a device for shifting the clock signal levels (FIG. 1-2, 7).

5. As to Claim 19, wherein the clock input of one of the end subassemblies is connected by means of an additional device for shifting the clock signal levels at the output of the clock circuit (FIG. 1-2, 7).

6. As to Claim 20, wherein the device for shifting the clock signal levels comprises at least one capacitor (¶ 21, 24).

7. As to Claim 21, wherein the device for shifting the clock signal levels comprises at least one transistor (FIG. 4-5).

8. As to Claim 22, wherein all the subassemblies are identical (FIG. 8: Elements 44-47 are identical in the sense all are transistors).

9. As to Claim 23, wherein each of the subassemblies comprises a voltage limiting circuit connected between its power supply terminals (FIG. 8, elements 44-47).

10. As to Claim 24, wherein the voltage limiting circuit comprises a diode (¶ 190).

11. As to Claim 25, wherein the voltage limiting circuit comprises a transistor (FIG. 8, elements 44-47).

12. As to Claim 27, wherein the integrated circuit comprises means for electrical insulation between the subassemblies (FIG. 8).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. **Claim 26 is rejected under 35 U.S.C. 103(a)** as being unpatentable over US Tamura in view of one or more of:

US Pub. No. 2003/0222698 to Khieu et al. (Khieu); and/or

US Pub. No. 2004/0085120 to Pitts (Pitts).

15. Tamura teaches substantially all of the limitations as stated above, except for a decoupling capacitor connected between the supply terminals.

16. Khieu discloses decoupling capacitor connected between the supply terminals (¶ 2), and Pitts discloses decoupling capacitor connected between the supply terminals (¶ 4).

17. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to have combined the teachings of Tamura with Khieu (¶ 2) and/or Pitts (¶ 4) to utilize a decoupling capacitor connected between the supply terminals, in order to reduce the noise on the power supply and ground lines (Khieu: ¶ 2) and/or protect the logic circuitry from transient voltage spikes and stabilize the supply voltage (Pitts: ¶ 4).

18. **Claim 28 is rejected under 35 U.S.C. 103(a)** as being unpatentable over Tamura in view of one or more of:

US Patent No. 5,594,261 to Temple (Temple);

US Patent No. 6,188,109 to Takahashi (Takahashi); and/or

US Pub. No. 2002/0014880 to McAndrews (McAndrews).

19. Tamura teaches substantially all of the limitations as stated above, except for the electrical insulation being reverse biased diode junctions.

20. Temple discloses electrical insulation being reverse biased diode junctions (Column 7, lines 2-9), Takahashi discloses electrical insulation being reverse biased diode junctions (Column 35, lines 50-64), and McAndrews discloses electrical insulation being reverse biased diode junctions (¶ 24).

21. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to have combined the teachings of Tamura with Temple (Column 7, lines 2-9), Takahashi (Column 35, lines 50-64), and/or McAndrews (¶ 24) to utilize reverse biased diode junctions for electrical insulation in order to free active area for signal lines and terminals (Temple: Column 7, lines 2-9), protect certain circuit components from the flow of current (Takahashi: Column 35, lines 50-64), and/or electrically isolate circuit components from each other (McAndrews: ¶ 24).

22. **Claim 29 is rejected under 35 U.S.C. 103(a)** as being unpatentable over Tamura in view of US Pub. No. 2002/0014663 to Iwamatsu et al. (Iwamatsu).

23. Tamura substantially teaches all of the limitations as stated above, except for dielectric zones.

24. Iwamatsu discloses dielectric zones (¶ 2).

25. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to have combined the teachings of Tamura with Iwamatsu (¶ 2) to utilize dielectric zones in order to obtain higher performance by isolating circuit elements (Iwamatsu: ¶ 2).

26. **Claim 30 is rejected under 35 U.S.C. 103(a)** as being unpatentable over Tamura in view of one or more of:

US Pub. No. 2004/0077151 to Bhattacharyya (Bhattacharyya),

US Pub. No. 2004/0087084 to Hsieh (Hsieh),

US Pub. No. 2004/0094763 to Agnello et al. (Agnello), and/or

US Pub. No. 2004/0018668 to Maszara (Maszara).

27. Tamura substantially teaches all of the limitations as stated above, except for silicon-on-insulator.

28. Bhattacharyya discloses silicon-on-insulator (Abstract; ¶ 4, 15), Hsieh discloses silicon-on-insulator (¶ 24), Agnello discloses silicon-on-insulator (¶ 49), and Maszara discloses silicon-on-insulator (¶ 2).

29. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to have combined the teachings of Tamura with Bhattacharyya (Abstract; ¶ 4, 15), Hsieh (¶ 24), Agnello (¶ 49), and/or Maszara (¶ 2) to utilize silicon-on-insulator in order to provide advantages of significant speed, power, and radiation immunity (Bhattacharyya: ¶ 4), reduce undesired capacitance (Maszara: ¶ 2), suppress short channel effect (Maszara: ¶ 2), and/or reduce latch-up and soft errors (Maszara: ¶ 2); since silicon-on-insulators are well-documented (Maszara: ¶ 2), well-known in the art (Hsieh: ¶ 24) and conventional (Bhattacharyya: Abstract; ¶ 15; Agnello: ¶ 49).

Response to Applicant Remarks

30. Applicant's remarks are moot in view of the new grounds of rejection.

Conclusion

31. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

32. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh Memula whose telephone number is (571) 272-8046. The examiner can normally be reached on M-F 8am-4:30pm EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

34. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Suresh Memula
Art Unit 2825
April 24, 2008

/Paul Dinh/
Primary Examiner, Art Unit 2825